

signal supplied to a gate thereof;

a1 a first bypassing means for bypassing a part of said input signal to a ground side according to the strength of said input signal; and

a second bypassing means for bypassing a part of said input signal to an output side according to the strength of said input signal.

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3. **(Amended)** A semiconductor integrated circuit as claimed in claim 2,

a2 wherein said first bypassing transistor is formed by M (M is an integer of 1 or more) transistors connected in series with each other such that a source of a transistor in a preceding stage is connected to a drain of a transistor in a succeeding stage; and

each of the gates of the M transistors is connected to said first bypass control voltage applying terminal via a resistance.

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5. **(Amended)** A semiconductor integrated circuit as claimed in claim 4,

a3 wherein said second bypassing transistor is formed by N (N is an integer of 1 or more) transistors connected in series with each other such that a source of a transistor in a preceding stage is connected to a drain of a transistor in a succeeding stage; and

each of the gates of the N transistors is connected to said second bypass control voltage applying terminal via a resistance.

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8. **(Amended)** A semiconductor integrated circuit as claimed in claim 6,

wherein a source of said signal amplifying transistor is grounded via a capacitance; and

said control means includes:

a4 a plurality of bias current controlling transistors whose drains are each connected to the source of said signal amplifying transistor and whose gates are connected to a plurality of drain bias current control voltage applying terminals via resistances; and

a plurality of self-bias resistances each having one end connected to one of the sources of said plurality of bias current controlling transistors, and each having another end connected to a reference potential.

11. **(Amended)** A radio communication apparatus comprising:

an antenna;

an AGC (Auto Gain Control) amplifier for amplifying a signal received by said antenna;

a mixer for mixing an output signal from said AGC amplifier with a predetermined frequency; and

a signal strength detecting circuit for detecting the signal strength of the received signal;

a5 said AGC amplifier including:

at least one signal amplifying transistor for

amplifying an input signal supplied to a gate thereof;

a first bypassing means for bypassing a part of said input signal to a ground side according to the strength of said input signal; and

a second bypassing means for bypassing a part of said

a5  
cont input signal to an output side according to the strength of said  
input signal.

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13. **(Amended)** A radio communication apparatus as claimed  
in claim 12,

wherein said first bypassing transistor is formed by M (M  
is an integer of 1 or more) transistors connected in series with  
each other such that a source of a transistor in a preceding  
stage is connected to a drain of a transistor in a succeeding  
stage; and

a6 each of the gates of the M transistors is connected to  
said first bypass control voltage applying terminal via a  
resistance.

14. **(Amended)** A radio communication apparatus as claimed  
in claim 12,

wherein said second bypassing means includes:

1 a second bypassing transistor having a drain connected to  
the drain of said first bypassing transistor and a gate connected  
to a second bypass control voltage applying terminal via a  
resistance; and

a second bias signal strength adjusting resistance having  
one end connected to a source of said second bypassing  
transistor, and another end connected to said bias voltage  
applying terminal via a resistance and connected to a drain of  
said signal amplifying transistor via a capacitance.

15. **(Amended)** A radio communication apparatus as claimed  
in claim 14,

wherein said second bypassing transistor is formed by N  
(N is an integer of 1 or more) transistors connected in series  
with each other such that a source of a transistor in a preceding  
stage is connected to a drain of a transistor in a succeeding  
stage; and